

Date Rev By History

Original AM69 SK’s PROC154E1/E2/E3_SCH with PDN-3H.1

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|------|------------|-----|--|
| V0.6 | 10/12/2022 | BMc | Initial capture J784S4 EVM Single Leo Dual HCPS PDN-3H.1 derived from PDN-3H v0.6 with following changes: 1. Removed In-line Safety FET to reduce cost & area 2. Removed Safety Voltage Supervisor 3. Removed Load Switch supplying VDD_IO_3V3 to SoC and updated Note 2. 4. Add SEL_3V3_1V8n control signal to PMIC’s GPIO6 from SoC GPIO to provison LDO2 to supply dual VIO for SD card HSD-I operation |
| V0.7 | 10/31/2022 | BMc | Added optional “PCle3_M2_SUSCLK” signal to be sourced from PMIC’s GPIO5 using 0ohm resistor and Note #13 description. Updated PDN title. |

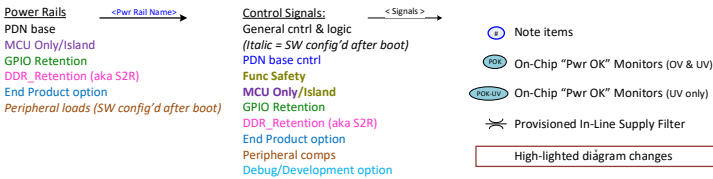
Latest AM69 SK’s PROC154E4_SCH with PDN-3H.IN v0.25

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|-------|-----------|-----|--|
| V0.25 | 7/23/2024 | BMc | Updated to latest 133A NVM v5 features and PDN changes by copying in J784S4 EVM PDN-3G v0.25 and applying all mods/revs as shown above for v0.6 & 0.7. |
|-------|-----------|-----|--|

Recommended PDN-3H.IN v0.32 for all new designs

| | | | |
|-------|------------|-----|--|
| | 9/3/2024 | BMc | Updated detailed Notes & PMC GPIO8 by adding optional PCle3_M.2_SUSCLK interface signal and note. |
| | 10/14/2024 | BMc | Updated PDN diag title & SoC block from J784S4” to “AM69” |
| V0.32 | 6/24/2025 | BMc | 1. Updated HCPS buck ENABLE inputs to more accurately show required 20k resistor located in-line to voltage translator output. 2. Updated Note 9's example #2 text & diag to show 20k resistor in-line with buck’s ENABLE inputs. |

Legend:



- Notes:
- An end product's Functional Safety desired ASIL target may require monitoring key "safety critical" power rails (i.e. VSYS_3V3 Input, key SoC supplies) that could cause severe system failures. This classification depends on the end product use case & what SoC resources a customer is using that are considered to be safety-related. SoC has internal OV & UV monitoring for key SoC MCU & Main voltage domains. The status is reported by SoC's Power OK (POK) status bits. Optional SoC voltage monitoring inputs (i.e. VMONx_IR_VEXTxx) can be used to extend SoC's OV/UV monitoring to a few board level power rails if desired (i.e. load switch Vo = VDD_IO_3V3). The following SoC Main & SDRAM domains are classified as non-critical & do not require direct monitoring: VDDSHV5 (SD Card), VPP_CORE, VPP_MCU, VDDA_3P3_USB & VDD1_LPDDR4_1V8.
 - Load Switches (LdSw) in-line with VSYS_3V3 can optional be removed to reduce PCB area & BOM cost depending upon an end product's system operation & desired features. Reasons to remove load switches from 3.3V power rails:
 - No latent fault protection is desired that could isolate any or all 3.3V SoC input supplies from a 1st power stage fault resulting in damage to SoC.
 - No system low power modes of operation (i.e. MCU Only, DDR Retention or GPIO Retention) are desired.
 - Full SoC PDN system power up & down sequences must be synchronized with enabling & disabling of the 1st power stage supplying VSYS_3V3 input.Enabling & disabling of SoC PDN must be executed with 1st power stage to avoid partially powering SoC for extended time periods that can negatively impact POH reliability. Reasons to use 3.3V load switches on 3.3V power rails:
 - Latent fault protection from 1st power stage that can avoid damaging SoC is desired.
 - Any one of the possible system low power modes of operation (i.e. MCU Only, DDR Retention or GPIO Retention) is desired.
 - Independent SoC power supply sequencing by PMIC resources ensures correct system start-up & shut-down timing delays per NVM settings.
 - Uncontrolled energizing of SoC 3.3V supplies is not recommended since this will partially power SoC for extended time periods that can negatively impact POH reliability.
 - PMIC's GPIO_8 has been provisioned to support multiple interface signals. The PMIC PN default function sets GPIO_8 = DISABLE_WDOG function following NVM initialization. This GPIO's default function can be reassigned by system SW following SoC boot if another interface signal is needed that is not required for SoC power sequencing.
 - Default: GPIO_8 = DISABLE_WDOG function to operate with EVM's DISABLE_WDOG signal that is latched on rising edge of PMIC's nRSTOUT = H_MCU_PORz_1V8 at end of power-up seq. A logic low enables normal watch dog timer operation while a logic high disables watch dog timer following a power up seq.
 - Option1: After system SW boots, SW can reassign GPIO_8 = GPI function to operate with PDN's MAIN_PWRGRP_IRQn (asserted high or low) signal. System SW must mask GPIO8 before changing GPIO8's assigned function. After selecting GPI function, SW must unmask GPI input and select whether the GPI will be either rising or falling edge sensitive. If any Main domain processing supply rail has a fault, the changing logic level on GPIO8 will set internal register bit that is monitored by PMIC's power state machine and cause a transition from Full Active state to MCU Safe state. At the board level, the WDOG_DISABLE & MAIN_PWRGRP_IRQn signals are "time mux'd" onto GPIO8's input pin by using a bi-state buffer with VDD_CORE_1V8. This enables WDOG_DISABLE not to set GPIO8's logic level during power up seq, H_MCU_PORz_1V8 = low since buffer is bi-stated. After power up seq, H_MCU_PORz_1V8 = high enabling buffer to drives MAIN_PWRGRP_IRQn logic level into GPIO8 input.
 - Option2: GPIO_8 = WKUP1 function can be selected by SW to operate with SoC's PMIC_PWR_EN1 signal for emulator debug control of PMIC power resources (i.e. enabling VDD_CORE to activate core logic required to support JTAG signaling across the device). Combining board level WDOG_DISABLE & PMIC_POWER_EN1 signals using a resistor network is possible since WDOG_DISABLE pulls logic level high when switch is closed. Afterwards, switch can be opened and PMIC_PWR_EN1 signal will drive GPIO_8.
 - GPIO Retention (aka GPIO_RET, IO_RET, IO_Wake) low power mode requires:
 - SoC SW executes command sequence that sets key PMIC register bits in order to enter GPIO_RET low power mode of operation and select the desired wake-up destination state (i.e. Full Active or MCU Only).
 - After entering GPIO_RET mode, the following power rails will remain energized & all other SoC MCU & Main supplies will be shut off to minimize power:
 - VDD_GPIORET_WK_OV8 supplying MCU's VDD_MCU_WAKE1 for MCU's 0.8V wake-up logic
 - VDD_GPIORET_IO_3V3 supplying MCU's VDDSHV0_MCU for MCU's 3.3V IO toggle activity
 - PDN system exits GPIO_RET state upon receiving logic toggles on SoC's MCU monitored IO signals ref to VDDSHV0_MCU supply. Then H_MCU_WAKE1n (= SoC's Open-Drain PMIC_WAKE1n, active low signal connected to PMIC, GPIO_4 (= WKUP1 default function for Full Active or = WKUP2 for MCU Only destination state) is asserted and PMIC state machine transitions PDN system to desired targeted wake up state.
 - The Open-Drain Buffer SN7ALVC16070R1 (tri-states IO when power is OFF) connects PMIC_WAKE1n to SoC_PWR_WKn net at discrete open-drain FET node. It is needed to isolate the SoC output buffer from the always on VCCA_3V3 used as pull-up supply to prevent current bleeding into SoC during low power modes (MCU Only, DDR_RET) when VDD_GPIORET_3V3 is typically disabled.
 - DDR Retention (aka DDR_RET, Suspend-to-RAM, S2R) low power mode requires:
 - At PMIC PN to assign GPIO_6 = Regulator Enable (RGEN) function with an open-drain output buffer type per NVM default settings. The board level net H_DDR_RET_1V1 signal is pulled up to VDD_DDR_1V1 & connected to SoC's DDR_RET input. When this input is set high, SoC's EMIF IO buffers are set to high-Z state as part of entering DDR_RET mode.
 - SoC SW executes command sequence that sets key PMIC register bits in order to enter DDR_RET low power mode of operation and select the desired wake-up destination state (i.e. Full Active or MCU Only).
 - After entering DDR_RET mode, the following power rails will remain energized & all other SoC MCU & Main supplies will be shut off to minimize power:
 - VDD_DDR_1V1 supplying both SoC EMIF & SDRAM IO voltages
 - VDD1_DDR_1V8 supplying SDRAM only
 - PDN system exits DDR_RET upon detecting a CAN_WAKE signal edge toggle on PMIC's GPIO_4 = LP_WKUP1 function per NVM settings that initiates exiting DDR_RET mode & restores Full Active processor operations.
 - SoC devices come in two types: General Purpose (GP) & High Security (HS). All GP devices can leave the VPP domains unconnected per DM. Pre-programmed HS devices can also leave VPP domains unconnected if no additional EFUSE programming is needed. If customer desires capability for in-the-field updates, then on-board EFUSE programming will require an additional 1.8V, 150mA LDO. When disabled, this LDO's Vo will need a high impedance output. Recommended PMIC: TPS73101-EP, fixed 1.8V TPS73118-Q1 or TLV70018-Q1. The EN_EFUSE_VPP control signal must be sourced from an SoC GPIO for this PDN (due to limited number of PMIC GPIOs). This allows SoC SW to control Efuse VPP voltage level by enabling & disabling dedicated LDO as needed to program High Security SoC Efuses (see SoC DM for details).
 - PDN shows SoC's VDDA_3P3_USB domain supplied from a low noise LDO with a VSYS_5V input as preferred for optimal USB 2.0 data eye mask performance. If USB 2.0 I/F is not used or is only needed for development tasks, then the digital VDD_IO_3V3 rail with in-line supply filter can be used as an alternate supply. Using digital VDD_IO_3V3 rail to support USB 2.0 I/F removes a discrete LDO & VSYS_5V input but could negatively impact data eye performance due to higher supply noise causing data eye mask violations.
 - PDN shows SoC's Main domain's VDDSHV5 supply being sourced from a dual voltage LDO with a VSYS_5V input as preferred for compliant high-speed SD card operation. If SD card is not used or only standard data rate operation is sufficient, then the digital VDD_IO_3V3 rail with in-line supply filter can be used as an alternate supply. Using digital VDD_IO_3V3 rail to support SD Card operation removes dual voltage, discrete LDO & VSYS_5V input but will restrict data rates to standard 12Mbps with VIO = 3.3V.
 - A discrete FET with low VGS (EVM uses industrial temp grade FET for low Vth) or single channel, voltage translation IC (automotive Q1 grade) can support low VIH needed to ensure a high level output will result with an input min 0.76V (-5% supply tol). If using SN74AXC145-Q1, please add a discrete FETs for an open-drain interface needed to interface with "MAIN_PWRGRP_IRQn" net. Examples shown below:

EVM Discrete FETs w/ low Vth

Auto Q1, Single Ch. Voltage Translator w/ FETs for open-drain interface
 - An optional "User I/F Push-Button" can be connected to PMIC GPIO_4 since a PMIC wake-up function & signal is not needed due to removal of all low power mode features. SW must write to PMIC to reassign GPIO_4's function to a GPI if this optional User I/F signal is desired.
 - An optional "Pcie3_M2_SUSCLK" signal can be sourced from PMIC's GPIO8 if needed for PCIe add-on cards in low power sleep modes. If ever used, system SW is needed to reassign GPIO8 function to CLK320UT to support this mode of operation. GPIO8 is used as a PMIC Resource Selection control signal which is pulled high to 3.3V supply during power up seq to direct PMIC resources to be configured for "Grouped PDN Type". After power up & system boot, GPIO8 function can be reassigned as needed.

Modular PDNs support flexible feature sets

| Feature Removals | Power Resource & Power Rail Removals | New Supply Mappings |
|-----------------------------------|--------------------------------------|--|
| HS SoC EFUSE Programming | Discrete LDO VPP_EFUSE_1V8 | SoC: VPP1 => No connects |
| Compliant, USB 2.0 data eye | Discrete LDO VDA_USB_3V3 | SoC: VDDA_3P3_USB => filtered VDD_IO_3V3 |
| Compliant, High-Speed SD Card | Discrete LDO VDD_SD_DIV | SoC: VDDSHV5 => VDD_IO_3V3 or VDD_IO_1V8 |
| DDR Retention low power mode | Discrete LDO VDD1_DDR_1V8 | LPDDR4: VDD1 => VDD_IO_1V8 |
| MCU GPIO Retention low power mode | Discrete LDO VDD_MCU_GPIORET_OV8 | Isolated MCU & Main PDN Schemes: SoC: VDD_MCU_WAKE1 => VDD_MCU_OV8S |
| | | Grouped MCU & Main PDN Schemes: SoC: VDD_MCU_WAKE1 => VDD_CORE_OV8 |
| | Discrete Ldsw VDD_MCU_GPIORET_3V3 | Isolated MCU & Main PDN Schemes: SoC: VDDSHV0_MCU => VDD_MCUIO_3V3 or VDD_MCUIO_1V8 |
| | | Grouped MCU & Main PDN Schemes: SoC: VDDSHV0_MCU => VDD_IO_3V3 or VDD_IO_1V8 |
| | Discrete SVS | PMIC: GPIO_10 pulled-up to VCCA_3V3 |
| | Discrete LDO VDD_GPIORET_OV8 | SoC: VDD_WAKE0 => VDD_CORE_OV8 |
| | Discrete Ldsw VDD_GPIORET_3V3 | SoC: VDDSHV2 => VDD_IO_3V3 or VDD_IO_1V8 |
| | Discrete SVS | PMIC: GPIO_10 pulled-up to VCCA_3V3 |

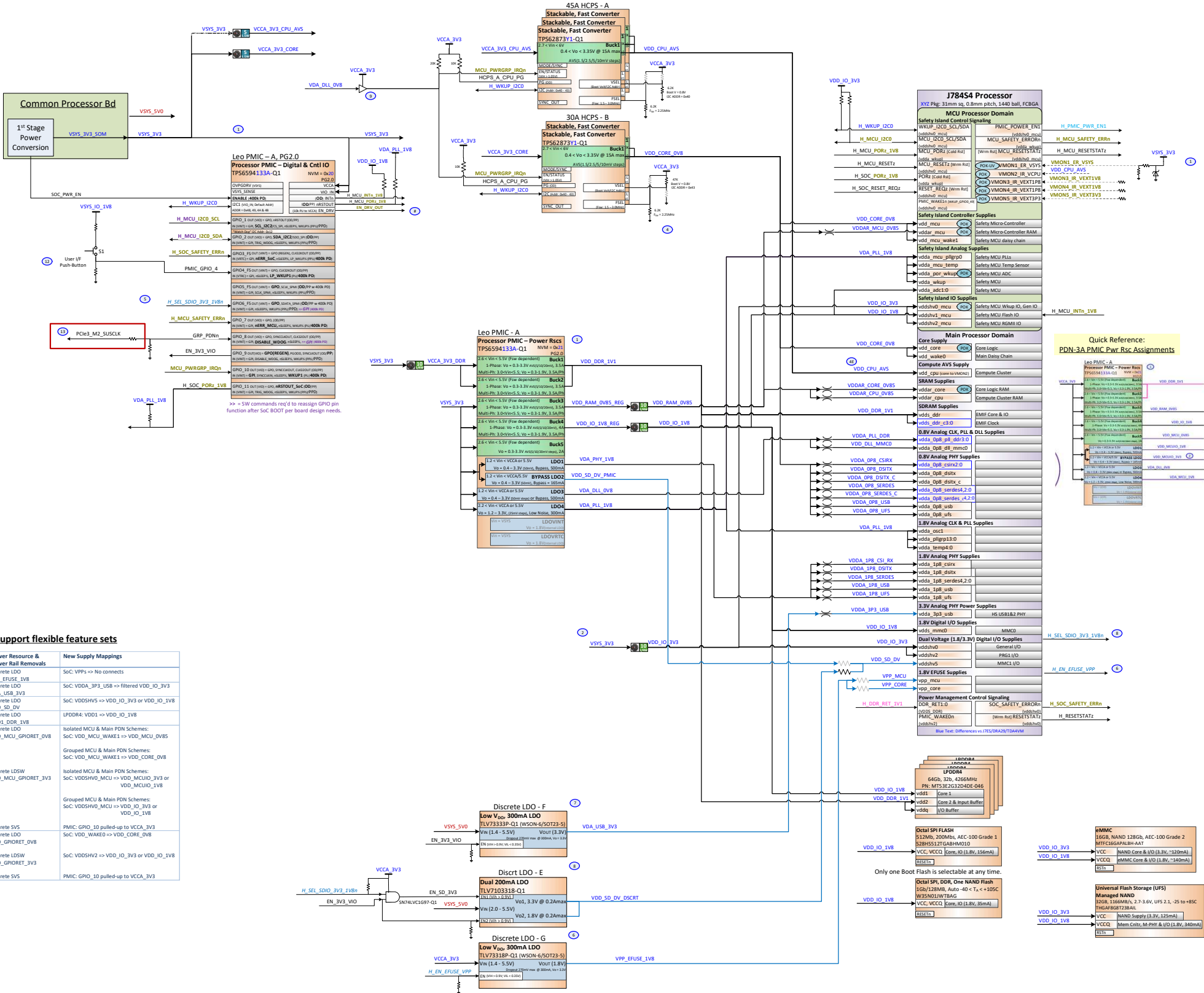
AM69 SK Leo + 2x High-Current Pwr Stages(HCPS) PDN-3H.1 (Power Rail & GPIO Mapping Overview)

Existing AM69 SK's PDN-3H.1

- V0.6 10/12/2022 BMC Initial capture J78454 EVM Single Leo Dual HCPS PDN-3H.1 derived from PDN-3H v0.6 with following changes:
- Removed In-line Safety FET to reduce cost & area
 - Removed Safety Voltage Supervisor
 - Removed Load Switch supplying VDD_IO_3V3 to SoC and updated Note 2.
 - Add SEL_3V3_1V8n control signal to PMIC's GPIO6 from SoC GPIO to provision LDO2 to supply dual VIO for SD card HS-I operation
- V0.7 10/31/2022 BMC Added optional "Pcie3_M2_SUSCLK" signal to be sourced from PMIC's GPIO5 using Dohm resistor and Note #13 description. Updated PDN title.

Features Supported (EVM Max Features):

- SoC performance: Max 2.0GHz clock with SERDES interfaces operational
- a. Not a Functional Safety capable sys
- b. Grouped Main & MCU power rails (no supply FFI)
- 4x SDRAMs: 32Gb, 4-Die, 32b, 4266MTs, LPDDR4 mode
- Boot & Mass Flash: Octal SPI or Hyperflash & eMMC, UFS
- Signaling Levels: MCU & Main Dual VIO
- End Product Options:
 - Compliant high-speed SD Card (needs 1 indep pwr rail & 1 VIO cntrl signal & discrete LDO needs Vin = 5V)
 - Compliant USB 2.0 data eye (needs 5V, 1 indep pwr rail & discrete LDO needs Vin = 5V)
 - HS SoC Efuse programming on-board (needs 1 indep pwr rail & 1 cntrl signal)



| Power Rails | Control Signals: | Note Items |
|---|---|--|
| <p>PDN base</p> <p>MCU Only/Safety Island</p> <p>GPIO Retention</p> <p>DDR_Retention (aka S2R)</p> <p>End Product option</p> <p>Peripheral loads (SW config'd after boot)</p> | <p>General cntl & logic (Italic = SW config'd after boot)</p> <p>PDN base cntl</p> <p>Func Safety</p> <p>MCU Only/Island</p> <p>GPIO Retention</p> <p>DDR_Retention (aka S2R)</p> <p>End Product option</p> <p>Peripheral comps</p> <p>Debug/Development option</p> | <p>On-Chip "Pwr OK" Monitors (OV & UV)</p> <p>On-Chip "Pwr OK" Monitors (UV only)</p> <p>Provisioned In-Line Supply Filter</p> <p>High-lighted diagram changes</p> |

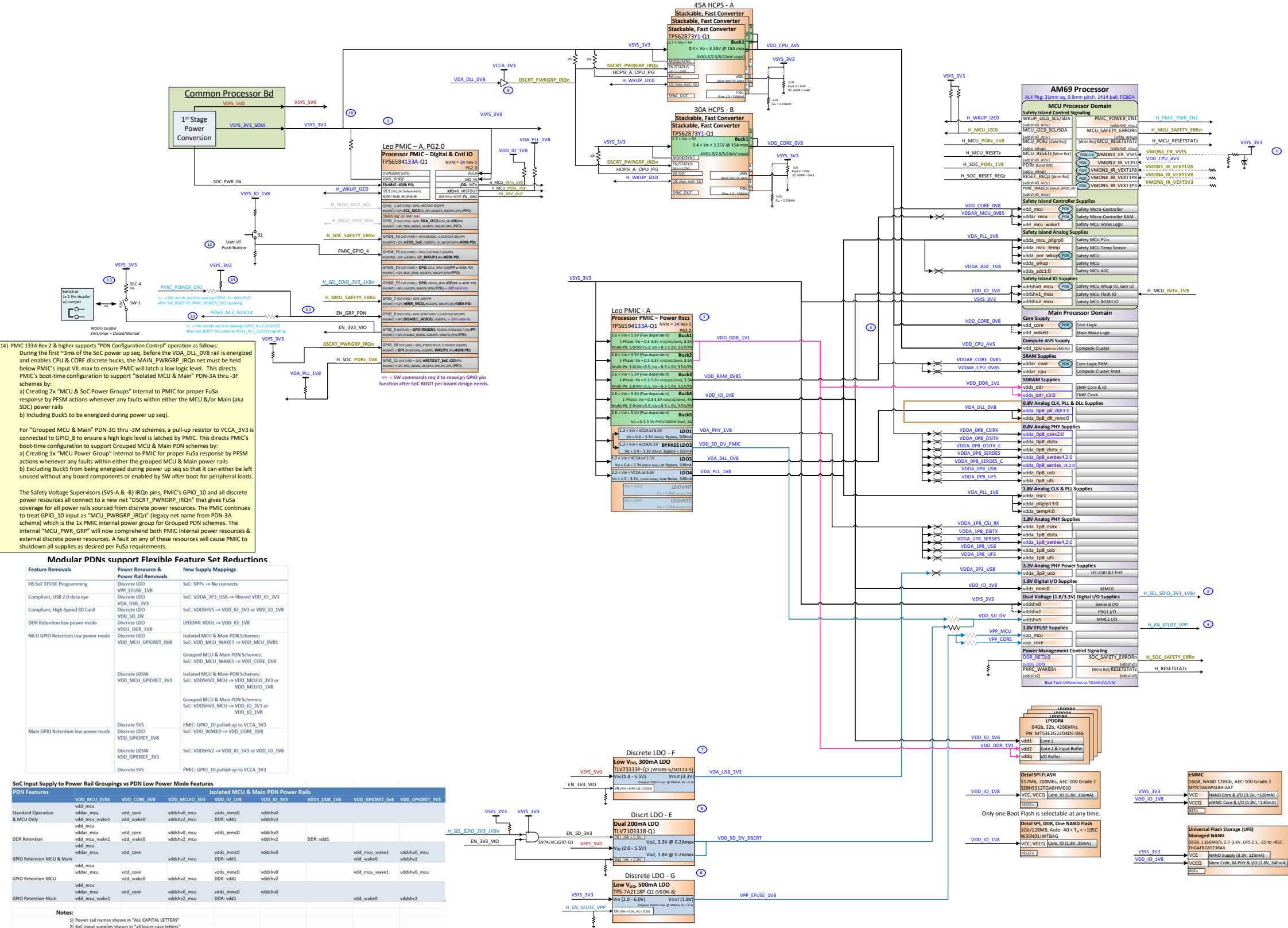
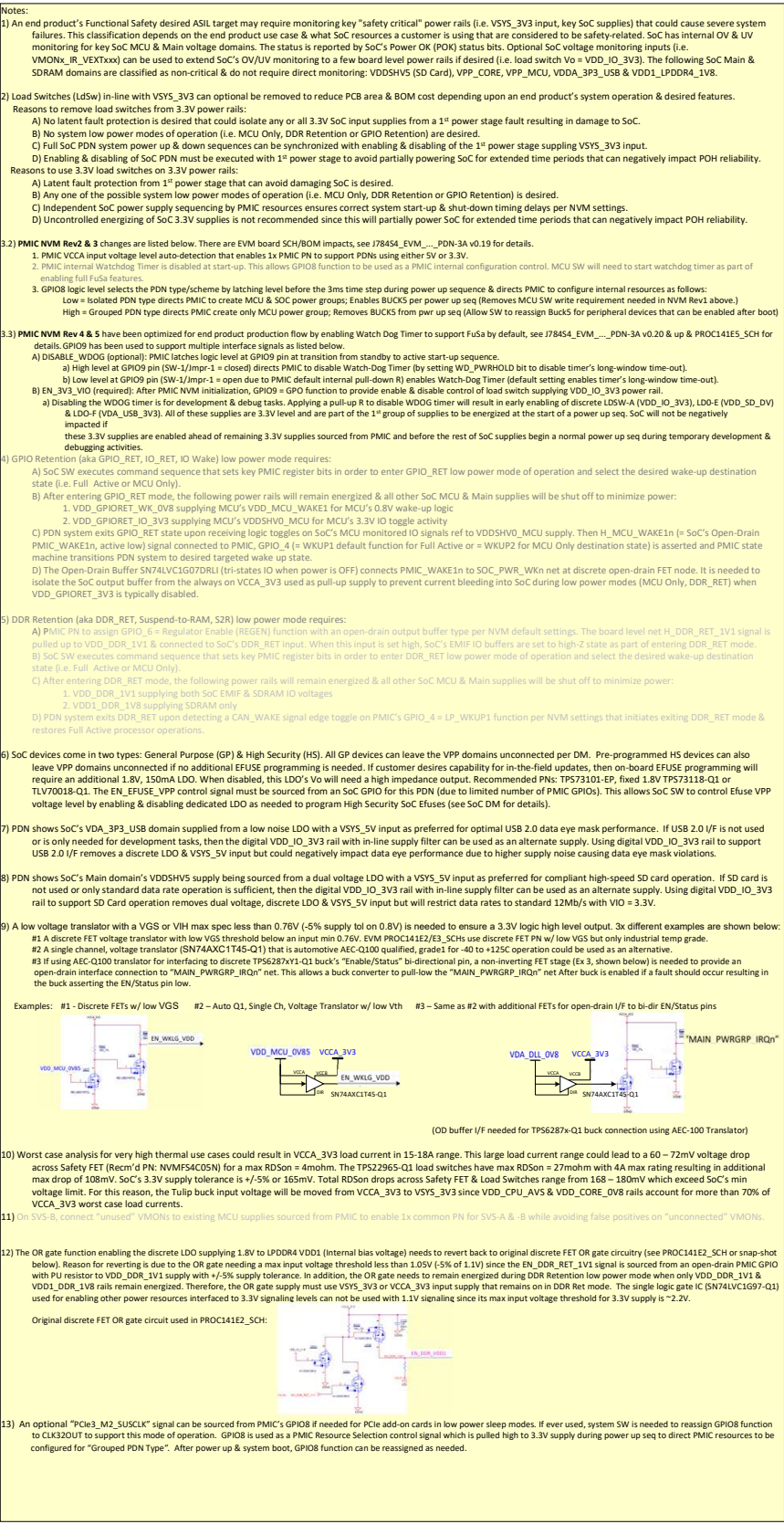
Not Applicable notes have "Greyed out" text.

Features Supported (EVM Max Features):

1. SoC performance: Max 2.0GHz clock with SERDES interfaces operational
2. **No Functional Safety**, Grouped Main & MCU power rails
3. 4x SDRAMs: 32Gb, 4-Die, 32b, 4266MT/s, LPDDR4 mode
4. Boot & Mass Flash: Octal SPI or Hyperflash & eMMC, UFS
5. Signaling Levels: MCU & Main Dual VIO
6. Low power modes:

- a. Compliant high-speed SD Card (needs 1 indep pwr rail & 1 VIO cntrl signal & discrete LDO needs Vin = 5V)
- b. Compliant USB 2.0 data eye (needs 5V, 1 indep pwr rail & discrete LDO needs Vin = 5V)
- c. HS SoC Efuse programming on-board (needs 1 indep pwr rail & 1 cntrl signal)

| Rev | Date | Desc |
|-------|------------|--|
| V0.25 | 6/24/2024 | 1. Updated PMIC 133A NVM rev to v5 per RTM planned revision and GPIO8 & 9 interface signals. |
| | 9/3/2024 | 2. Updated detailed Notes & PMC GPIO8 by adding optional PCIe3_M.2_SUSCLK interface signal and note. |
| | 10/14/2024 | 3. Updated PDN diag title & SoC block from J78454" to "AM69" |



| Power Rails | <Pwr Rail Name> | Control Signals: | <Signals> | | Note items |
|---|-----------------|--|-----------|---|-------------------------------------|
| PCN base | | General ctrl'l & logic | | | |
| MCU Only/Safety Island | | <i>(Italic = SW config'd after boot)</i> | | | |
| GPIO Retention | | PCN base ctrl'l | |  | On-Chip "Pwr OK" Monitors (OV & UV) |
| DDR_Retention (aka S2R) | | Func Safety | | | |
| End Product option | | MCU Only/Island | |  | On-Chip "Pwr OK" Monitors (UV only) |
| Peripheral loads (SW config'd after boot) | | GPIO Retention | | | |
| | | DDR_Retention (aka S2R) | |  | Provisioned In-Line Supply Filter |
| | | End Product option | | | |
| | | Peripheral comps | | | |
| | | Debug/Development option | | | |
| | | | | | High-lighted diagram changes |

Not Applicable notes have "Greyed out" text.

Features Supported (EVM Max Features):

1. SoC performance: Max 2.0GHz clock with SERDES interface
2. **No Functional Safety**, Grouped Main & MCU power rails
3. 4x SDRAMs: 32Gb, 4-Die, 32b, 4266MT/s, LPDDR4 mode
4. Boot & Mass Flash: Octal SPI or Hyperflash & eMMC,
5. Signaling Levels: MCU & Main Dual VIO
6. Low power modes:

7. End Product Options:

- a. **Compliant high-speed SD Card** (needs 1 indep pwr rail & 1 VIO cntrl signal & discrete LDO needs Vin = 5V)
- b. **Compliant USB 2.0 data eye** (needs 5V, 1 indep pwr rail & discrete LDO needs Vin = 5V)
- c. **HS SoC Efuse programming on-board** (needs 1 indep pwr rail & 1 cntrl signal)

Note: All new product designs should align to PDN-3H.IN v0.32 or latest version.

| Rev | Date | Desc |
|-------|-----------|---|
| V0.32 | 6/24/2025 | <ol style="list-style-type: none">1. Updated HCPS buck ENABLE inputs to more accurately show required 20k resistor located in-line to voltage translator output.2. Updated Note 9's example #2 text & diag to show 20k resistor in-line with buck's ENABLE inputs. |

2. Latency switches (LdSw) in-line with VSV5_3v3 can optional be removed to reduce PCB area & BOM cost depending upon an end product's system operation & desired features.

Reasons to avoid latent fault switches from 3.3V power rails:

- A) Latent fault fault switch is desired that could isolate any or all 3.3V SoC input supplies from a 1st power stage fault resulting in damage to SoC.
- B) No system low power modes of operation (i.e. MCU Only, DDR Retention or GPIO Retention) are desired.
- C) Full SoC PDM system power up & down sequences can be synchronized with enabling & disabling of the 1st power stage supplying VSV5_3v3 input.
- D) Latency & disabling of the 3.3V power stage with 1st power stage to avoid partially powering SoC for extended time periods that can negatively impact POH reliability.

Reasons to use 3.3V latent fault switches on 3.3V power rails:

- A) Latent fault protection from 1st power stage that can avoid damaging SoC is desired.
- B) Any one of the possible system low power modes of operation (i.e. MCU Only, DDR Retention or GPIO Retention) is desired.
- C) Latent fault protection SoC power sequencing by PMIC resources enables correct system start-up & shut-down similar to delay or NVM settings.
- D) Uncontrolled energizing of SoC 3.3V supplies is not recommended since this will partially power SoC for extended time periods that can negatively impact POH reliability.

3) **PMIC NVN Rev 4.5** has been optimized for end product production flow by enabling Watch Dog Timer to support fuses by default, see j78454_EVN..._PDN-v3.0 v2.0.8 and PROC14155_SCH for details. GP02D has been used to support multiple interface signals as listed below:

- a) **GP02D_VDD (logic)** enables logic level at GP02D pin at transition from standby to active start-up sequence.
- b) **High level at GP02D pin (SW-1/Imp-1)** - closed directs PMIC to disable Watch-Dog timer (by setting WD_PVRHOLD bit to disable timer's long-window timeout mode).
- c) **Low level at GP02D pin (SW-1/Imp-1)** - open due to PMIC default setting (input pull-down) enables Watch-Dog timer (default setting enables timer's long-window timeout mode).
- d) **GP02D_VDD (required)** - enables PMIC to disable control of the Watch-Dog timer. This signal is disabled control of the Watch-Dog timer by setting the bit DISWDG_VDD to 1.
- e) **Disabling VDDG timer** for development & debug tasks. Applying a pull-up to R12 to disable WDOG timer will result in early enable of discrete LSI2W4 (VDD_0_V3V3, LDO2-[VDD_SD_VD]) and LDO2-[VDD_SD_V3V3]. All of these supplies are 3.3V level and are part of the 1st group of supplies to be energized at the start of a power up seq. So, will not be negatively impacted if

these 3.3V supplies are enabled ahead of remaining 3.3V supplies sourced from PMIC and before the rest of SoC supplies begin a normal power up seq during temporary development and debugging activities.

DDR Retention (aka DDR_RET, Suspect-to-RAM, S2R) low power mode requires:

- A) **Phy** must be in **drain** output buffer type for NVm default settings. The board level **DDR_RET, DDR_RET_1V1** signal is pulled up to **VDD, DDR_1V1** and connected to **SoC's DDR_RET** input. When this input is high, **SoC's** EMIF buffers are set to high-Z state after entering **DDR_RET** mode.
- B) **SoC SW** executes command sequence that sets key PMIC register bits in order to enter **DDR_RET** low power mode of operation and select the desired wake-up destination state (i.e. Full Active or MCU Only).
- C) After entering **DDR_RET** mode, the following power rails will remain energized & all other SoC MCU & Main supplies will be shut off to minimize power:
 - 1. **VDD, DDR_1V1** supplying both SoC EMIF & SDRAM I/O voltages
 - 2. **VDD1, DDR_1V8** supplying SDRAM only
- D) PDn system exits **DDR_RET** upon detecting a CAN, WAKE signal edge toggle on PMIC's **GPI0_4 = LP_WKUP1** function per NVm settings that initiates exiting **DDR_RET** mode & restores Full Active processor operations.

3) PDN shows SoC's Main domain's VDDSHV5 supply being sourced from a dual voltage LDO with a VSYS_5V input as preferred for compliant high-speed SD card operation. If SD card is not used or only standard data operation is sufficient, then the digital VDD_IO_3V3 rail with in-line supply filter can be used as an alternate supply. Using digital VDD_IO_3V3 rail to support SD Card operation removes dual voltage, discrete LDO & VSYS_5V input but will restrict data rates to standard 12Mb/s with VIO = 3.3V.

Examples: #1 - Discrete FETs w/ low VGS #2 – Auto Q1, Single Ch, Voltage Translator w/ low Vth #3 – Same as #2 with additional FETs for open-drain I/F to bi-dir EN/Status pins

The diagram shows three circuit examples for driving a relay coil from a microcontroller pin.

Example #1: A discrete MOSFET driver circuit. The microcontroller pin (VDA_D1L_0V8) drives the gate of a MOSFET (Q1). The MOSFET's source is grounded, and its drain is connected to one terminal of a relay coil. The other terminal of the relay coil is connected to VCCA_V3V3. A pull-up resistor (R1) connects the microcontroller pin to VCCA_V3V3. The label "MAIN_PWRGRG_IRQn" is shown near the relay coil.

Example #2: An automatic level-shifting circuit. The microcontroller pin (VDA_D1L_0V8) drives the gate of a MOSFET (Q1). The MOSFET's source is connected to the drain of another MOSFET (Q2), which has its gate tied to VCCA_V3V3 and its source grounded. The drain of Q2 is connected to one terminal of the relay coil. The other terminal of the relay coil is connected to VCCA_V3V3. A pull-up resistor (R1) connects the microcontroller pin to VCCA_V3V3. The label "MAIN_PWRGRG_IRQn" is shown near the relay coil.

Example #3: Similar to Example #2, but includes an additional MOSFET (Q3) for open-drain functionality. The microcontroller pin (VDA_D1L_0V8) drives the gates of both Q1 and Q3. Q1's source is connected to the drain of Q3, which has its gate tied to VCCA_V3V3 and its source grounded. Q1's drain is connected to one terminal of the relay coil. The other terminal of the relay coil is connected to VCCA_V3V3. A pull-up resistor (R1) connects the microcontroller pin to VCCA_V3V3. The label "MAIN_PWRGRG_IRQn" is shown near the relay coil.

(OD buffer I/F needed for TP56287X-Q1 buck connection using AEC-100 Translator)

12) The OR gate function enabling the discrete D0R supply 1.8V to LPD0R4D01 (internal bias voltage) needs to revert back to original discrete RET_FET OR gate circuitry (see PHOC14122_5CH or snap-shot below). Reason for reverting is due to the OR gate needing a max input voltage threshold less than 1.05V (5% of 1.1V) since the OR_GATE_RET signal is sourced from an open-drain PMIC P0R0 with PU resistor to VDD_0R1 supply with +1.5% supply tolerance. In addition, the OR gate needs to remain energized during D0R Retention low power mode when only VDD_0R1, D0R_1, and VDD01_D0R1, VDD01_0R1 rails remain energized. Therefore, the OR gate supply must use VY55_3V3 or VCCA_3V3 supply that remains on in D0R Ret mode. The single logic gate IC (SN74VLC01697-01) used for enabling other power resources interfaced to 3.3V signal. 1V signaling is its max input voltage threshold for 3.3V supply is +2.4V.

Original discrete FET OR gate circuit used in PROC141E2_SCH:

13) An optional "PCIE3_M2_SUSCLK" signal can be sourced from PMIC's GPIO8 if needed for PCIe add-on cards in low power sleep modes. If ever used, system SW is needed to reassign GPIO8 function to CLK32OUT2 to support this mode of operation. GPIO8 is used as a PMIC Resource Selection control signal which is pulled high to 3.3V supply during power up seq to direct PMIC resources to be configured for "Grouped PDN Type". After power up & system boot, GPIO8 function can be reassigned as needed.

